Abstract

A system that allows an end user to optimize the performance of a logic analyzer quickly and easily is disclosed. A visual display allowing a user to see a data valid window and relative sample positions is provided. Direct graphical manipulation of the sample position allows for quick and accurate setting of sample positions. The present invention provides a graphical user interface generally comprised of the following components: a stable and transitioning data display; bus/signal labels; sample position time scale; an information icon; a timestamp icon; a graphical representation of suggested and selected sample position; a text display of selected sample position; and a legend. The present invention sets up the logic analyzer to correctly sample data from high speed, low margin systems. It measures data signals from the device under test relative to the user's state clock and automatically suggests the sampling position offset for each channel of the analyzer. The present invention allows the user to accept the suggestions or select alternative sampling positions manually.